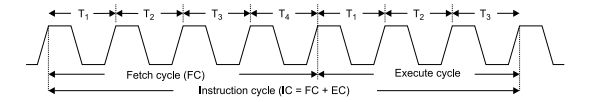
**1. Instruction cycle:** It is defined as the number of steps required by the CPU to complete the entire process i. e. Fetching and execution of one instruction. The fetch and execute cycles are carried out in synchronization with the clock.

i.e .IC is the total time required to execute an instruction completely.

**2. Machine cycle:** It is the time required by the microprocessor to complete the operation of accessing the memory devices or I/O devices. In machine cycle various operations like opcode fetch, memory read, memory write, I/O read, I/O write are performed.

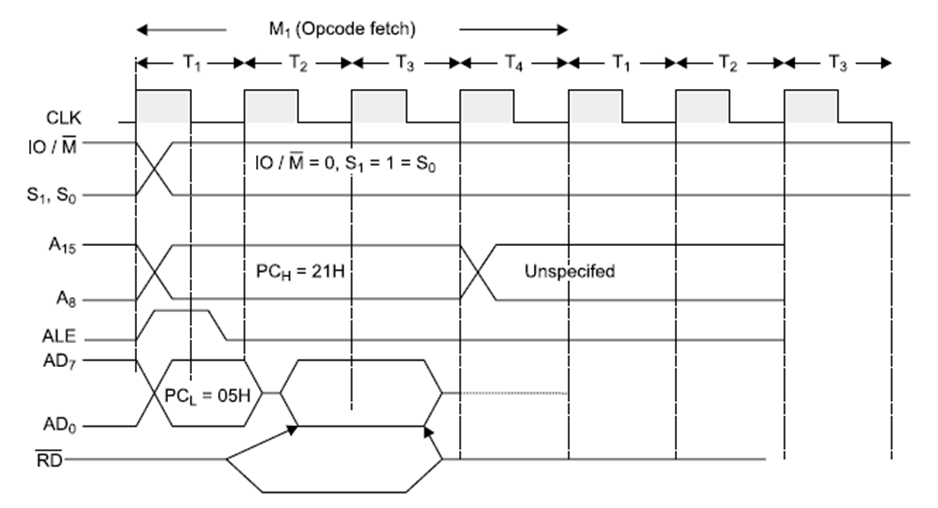
**3. T-state:** Each clock cycle is called as T-states.

**Rules to identify number of machine cycles in an instruction:**  
1. If an addressing mode is direct, immediate or implicit then No. of machine cycles = No. of bytes.  
  
2. If the addressing mode is indirect then No. of machine cycles = No. of bytes + 1. Add +1 to the No. of machine cycles if it is memory read/write operation.  
  
3. If the operand is 8-bit or 16-bit address then, No. of machine cycles = No. of bytes +1.  
  
4. These rules are applicable to 80% of the instructions of 8085.

**Timing Diagram:**  


Where, Instruction cycle = Fetch Cycle (FC) + Execute cycle (EC).

**Opcode fetch:**

 The microprocessor requires instructions to perform any particular action. In order to perform these actions microprocessor utilizes Opcode which is a part of an instruction which provides detail (ie. Which operation µp needs to perform) to microprocessor.*Fig: Opcode fetch timing diagram*

**Operation:**

 During T1 state, microprocessor uses IO/M(bar), S0, S1 signals are used to instruct microprocessor to fetch opcode.

 Thus when IO/M(bar)=0, S0=S1= 1, it indicates opcode fetch operation.

 During this operation 8085 transmits 16-bit address and also uses ALE signal for address latching.

 At T2 state microprocessor uses read signal and make data ready from that memory location to read opcode from memory and at the same time program counter increments by 1 and points next instruction to be fetched.

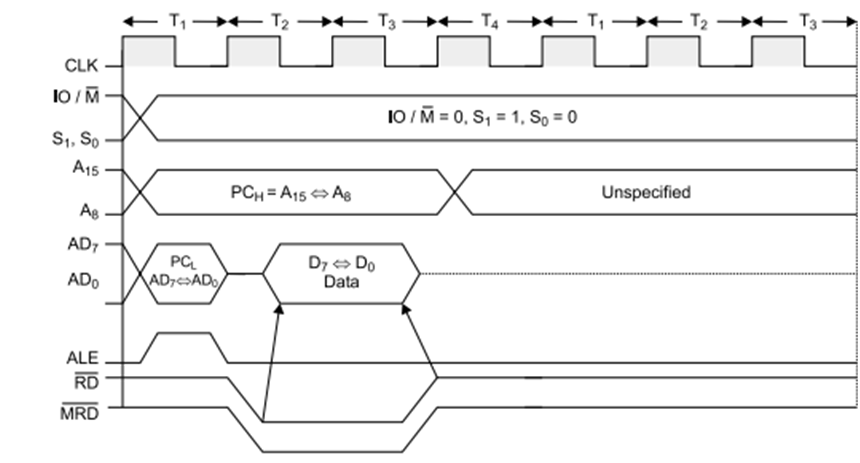
 In this state microprocessor also checks READY input signal, if this pin is at low logic level ie. '0' then microprocessor adds wait state immediately between T2 and T3.

 At T3, microprocessor reads opcode and store it into instruction register to decode it further.

 During T4 microprocessor performs internal operation like decoding opcode and providing necessary actions.

 The opcode is decoded to know whether T5 or T6 states are required, if they are not required then µp performs next operation.

**Read and write timing diagram for memory and I/O Operation**

**Memory Read:** <>Figure: Memory read timing diagram

**Operation:**

 It is used to fetch one byte from the memory.

 It requires 3 T-States.

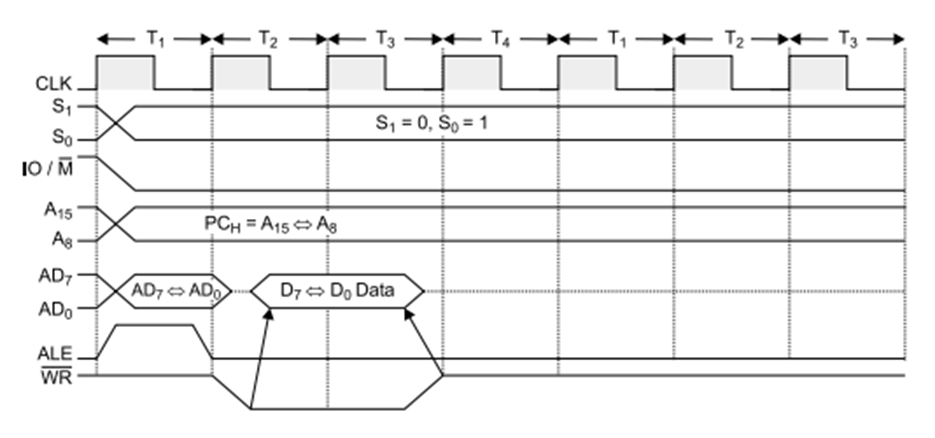
 It can be used to fetch operand or data from the memory.

 During T1, A8-A15 contains higher byte of address. At the same time ALE is high. Therefore Lower byte of address A0-A7 is selected from AD0-AD7.

 Since it is memory ready operation, IO/M(bar) goes low.

 During T2 ALE goes low, RD(bar) goes low. Address is removed from AD0-AD7 and data D0-D7 appears on AD0-AD7.

 During T3, Data remains on AD0-AD7 till RD(bar) is at low signal.

**Memory Write:** *Figure: Memory write timing diagram*

**Operation:**

 It is used to send one byte into memory.

 It requires 3 T-States.

 During T1, ALE is high and contains lower address A0-A7 from AD0-AD7.

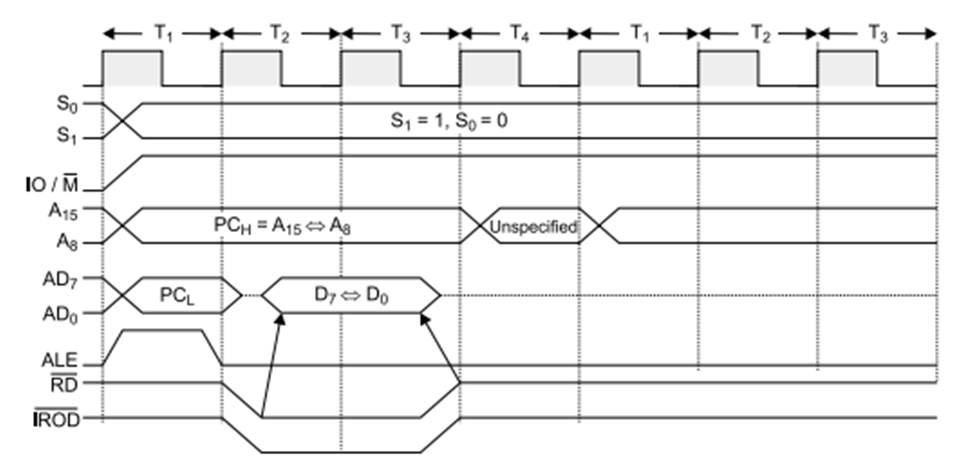
 A8-A15 contains higher byte of address

.

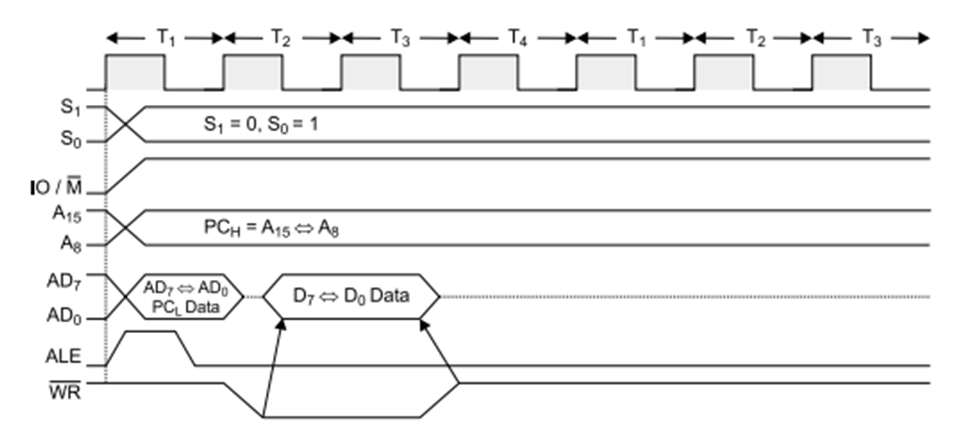
 As it is memory operation, IO/M(bar) goes low.

 During T2, ALE goes low, WR(bar) goes low and Address is removed from AD0-AD7 and then data appears on AD0-AD7.

 Data remains on AD0-AD7 till WR(bar) is low.

**IO Read:** *Figure: I/O read timing diagram*

**Operation:**   
  
It is used to fetch one byte from an IO port.  
  
  
It requires 3 T-States.  
  
  
During T1, The Lower Byte of IO address is duplicated into higher order address bus A8-A15.  
  
  
ALE is high and AD0-AD7 contains address of IO device.  
  
  
IO/M (bar) goes high as it is an IO operation.  
  
  
During T2, ALE goes low, RD (bar) goes low and data appears on AD0-AD7 as input from IO device.  
  
  
During T3 Data remains on AD0-AD7 till RD (bar) is low.

**IO Write:** Figure: I/O write timing diagram

**Operation:**

 It is used to writ one byte into IO device.

 It requires 3 T-States.

 During T1, the lower byte of address is duplicated into higher order address bus A8-A15.

 ALE is high and A0-A7 address is selected from AD0-AD7.

 As it is an IO operation IO/M (bar) goes low.

 During T2, ALE goes low, WR (bar) goes low and data appears on AD0-AD7 to write data into IO device.

 During T3, Data remains on AD0-AD7 till WR(bar) is low..